Radiation Tolerance Evolution of CMOS Integrated Circuits

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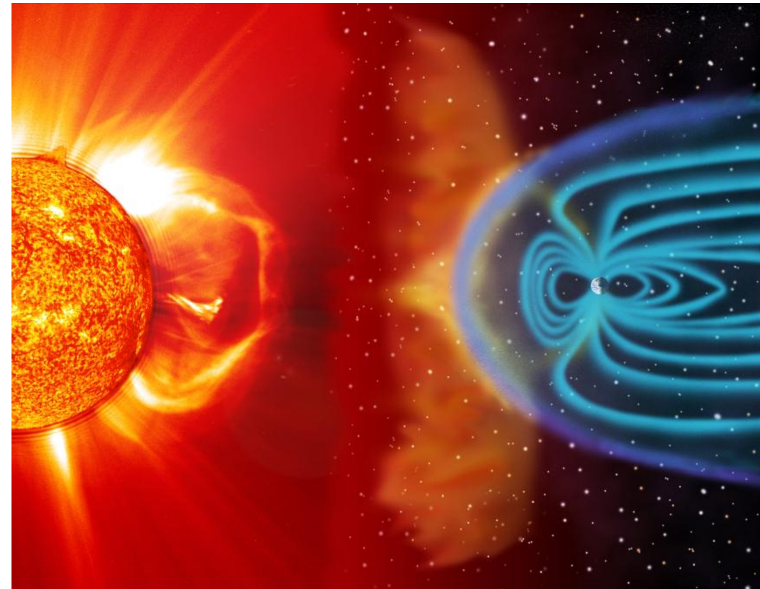
INVAP

"η γνώση θα σας απελευθερώσει"
(*knowledge will set you free*) .
SOCRATES

INTRODUCTION

Technology	10 µm	3 µm	1.5 µm	1 µm	800 nm	600 nm	350 nm	250 nm	180 nm		130 nm	90 nm	65 nm	45 nm	32 nm	28 nm	22 nm	FINFET 14 nm	FD-SOI 28/22 nm		10 nm	7 nm	5 nm
Year	1971	1975	1982	1985	1989	1994	1995	1997	1999	2000	2002	2004	2006	2008	2010	2011	2012	2014	2015	2016	2017	2018	2020

- Radiation: Main concern in space missions
- CMOS technology TID/ SEU/SEL susceptible
- Moor’s Law
- Effects Scale Integration

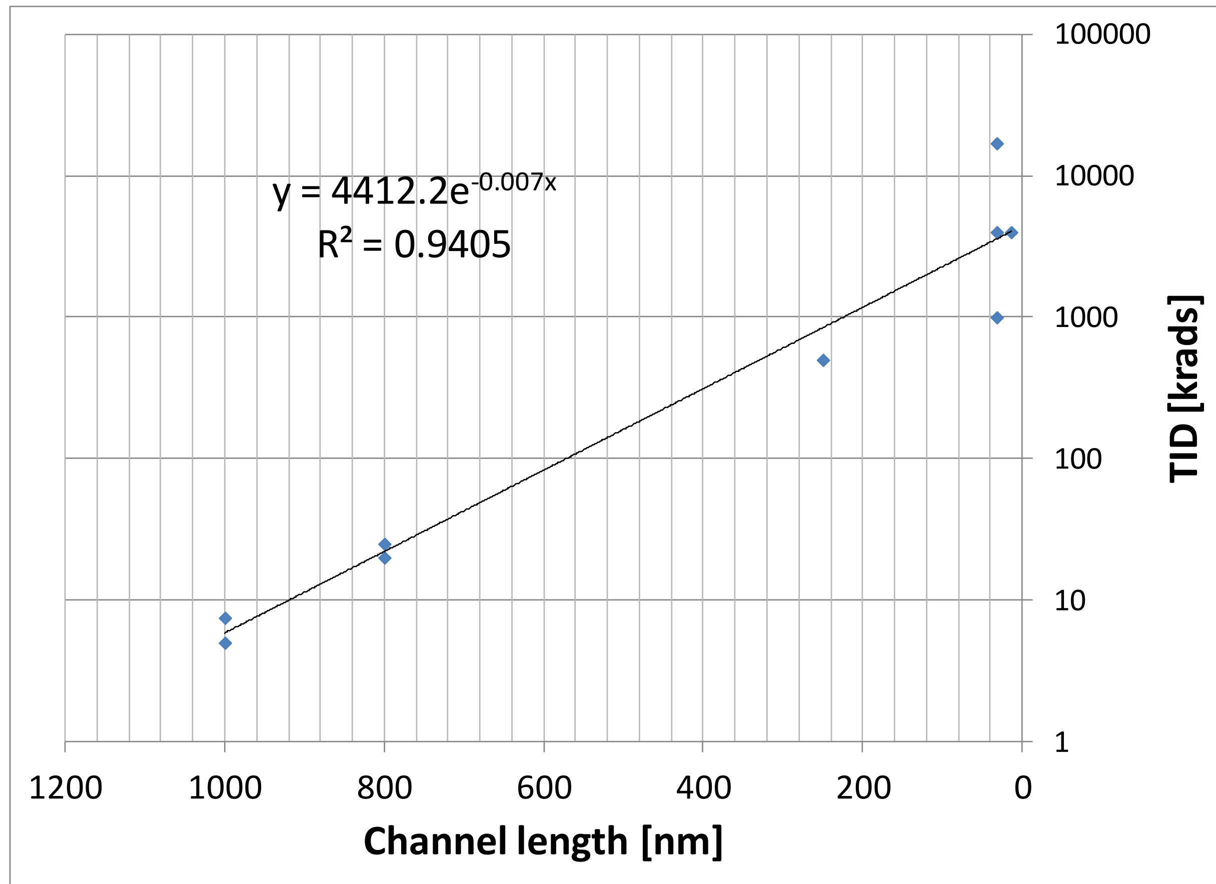


(Total Ionizing Dose)

TID and Technology Evolution

MANUFACTURER	DEVICE	TECHNOLOGY [nm]	TEST DATE	RESULT [krads (Si)]	REFERENCE
INTEL	80386-20	1000	1993	5 to 7.5	[1, 4, 5]
INTEL	80486DX2-66	800	1995	20 to 25	[2, 4, 5]
INTEL	PENTIUM III	250	2000-2	~ 500	[3, 4, 5]
AMD	K7	180	2002	> 100	[3, 4, 5]
AMD	Llano	32	2013	1000, 4000, 17000	[4]
INTEL	Core™ i3-5005U	14	2015	4000	[4]

TID and Technology Evolution



Why does Total Dose tolerance increase with technology?

$$\Delta V_{OT} = -\frac{q}{C_{OX}}\Delta N_{OT} = -\frac{q}{\varepsilon_{OX}} d_{OX} \cdot \Delta N_{OT}$$

$$C_{OX} = \frac{\varepsilon_{OX}}{d_{OX}}$$

$$\Delta V_{OT} \approx d_{OX}^{\ 2}$$

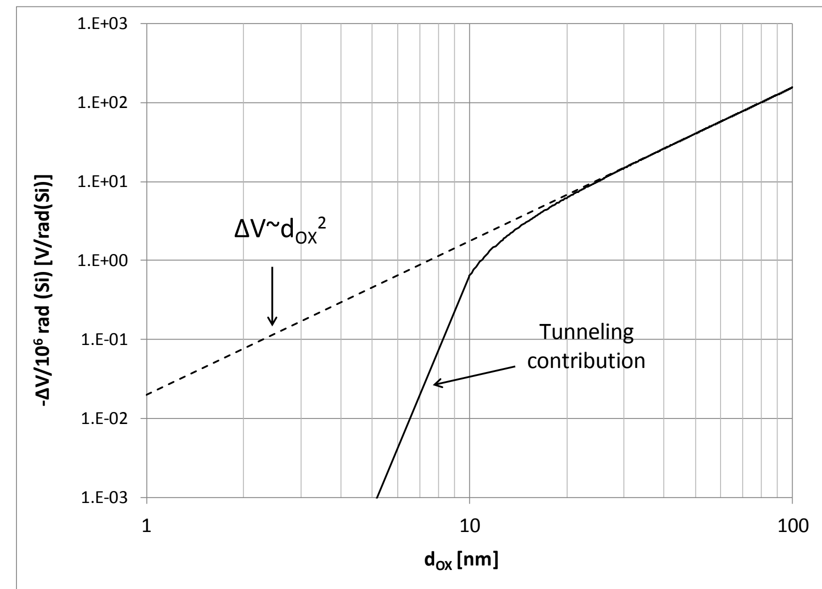
q: elementary charge (1.6x10-19 C)

C_{OX} = specific capacitance of the MOS capacitor [F/m^2]

d_{OX}: gate oxide thickness

ε_{OX}: dielectric constant

ΔN_{OT}: density of oxide trapped holes per area unit [m^{-2}]



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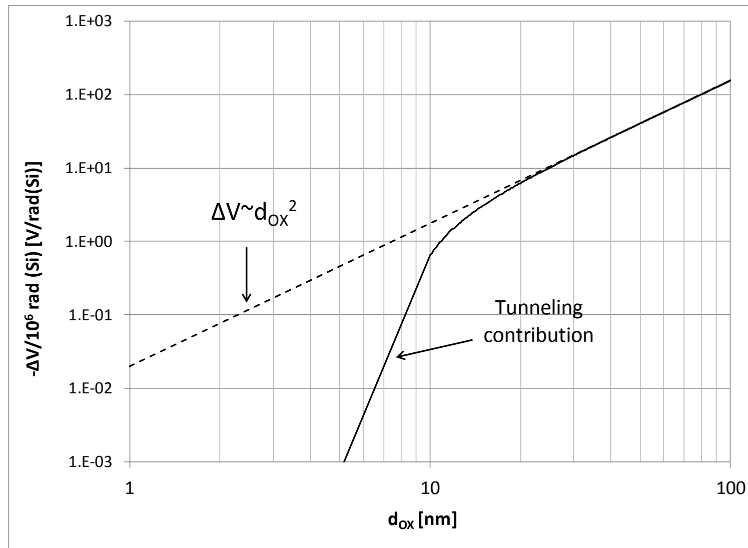
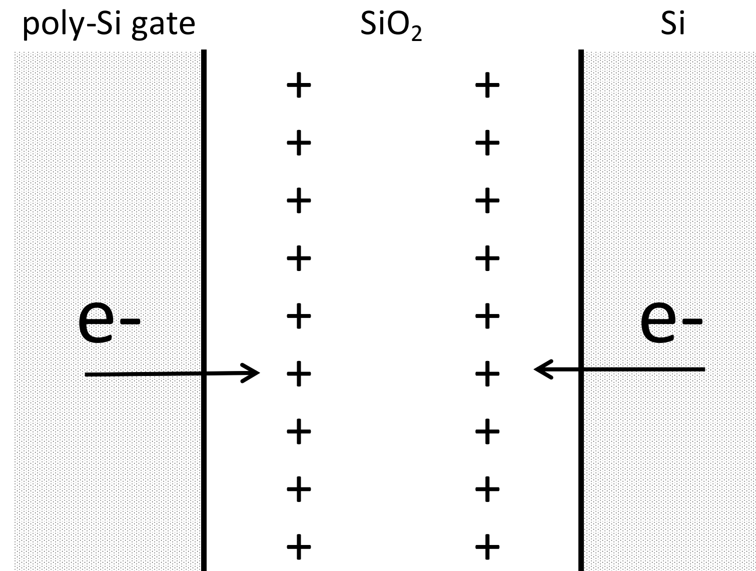
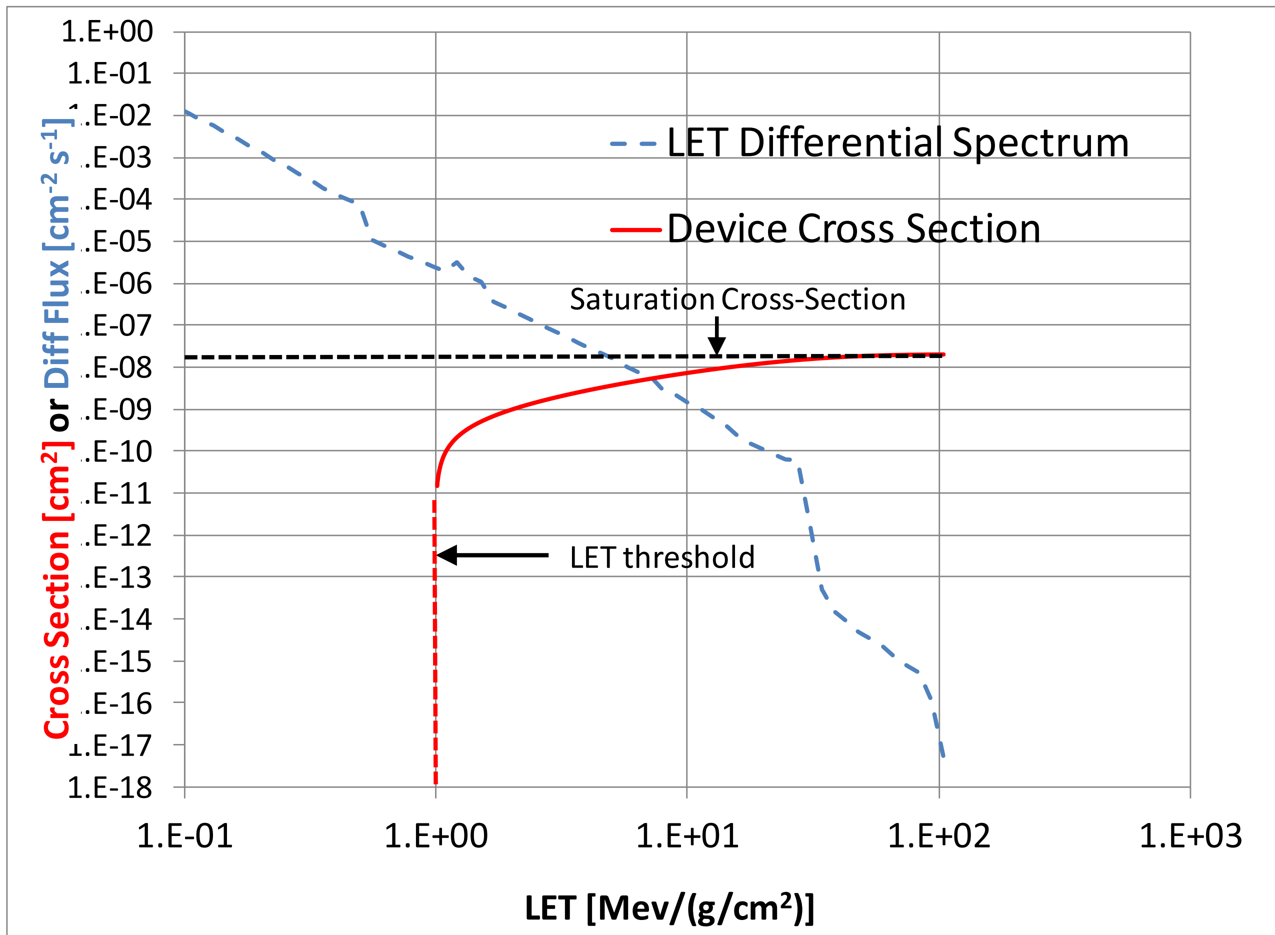




Effect of the Fowler-Nordheim tunneling transport mechanism

SEU/SEFI

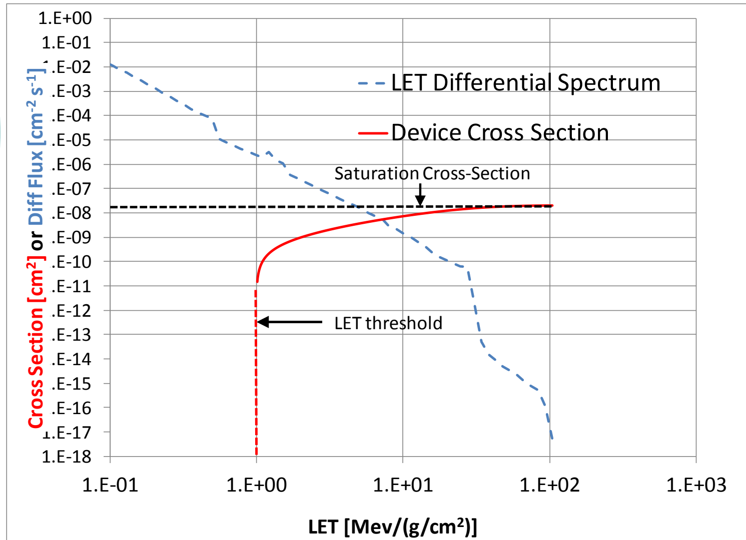
CROSS-SECTION AND LET SPECTRUM

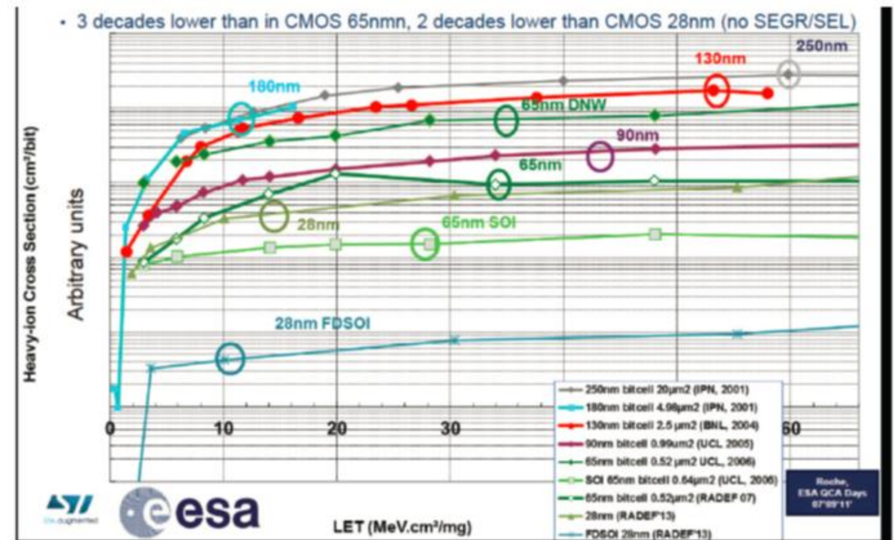


SEU/SEFI (soft errors) [6]

ORBIT	555.6 Km	57°	circular	2.5" Al shielding	
PROCESSOR	**Technology**	**Channel Length [μm]**	**Upset Cross Section [cm^2/device]**	**LETth [$MeV/mg/cm^2$]**	**Upset Rate [per day]**
8086	NMOS	3	$1x10^{-3}$	0.2	0.0511
80C86	CMOS	3	$4x10^{-3}$	1	0.0120
80186	NMOS	1.5	$0.4x10^{-4}$	0.4	$6.01x10^{-4}$
80186	CHMOSIII	1.5	$1x10^{-3}$	9	$6.27x10^{-5}$
80386	CHMOSIV	1.5	$1x10^{-3}$	3.4	$3.50x10^{-4}$
80486	CMOSIV	0.8	$2x10^{-4}$	3	$8.72x10^{-5}$
80486	CMOSV	0.8	$2x10^{-4}$	5	3.54x10-[5]
Pentium 150 MHz	BICMOS	0.35	$1x10^{-4}$	3.5	$3.32x10^{-5}$
MMX	CMOS	0.28			0.00129

Soft Errors Evolution ANALYSIS [7]





$$Qcrit \cong Cnode \cdot VDD$$

$$LETthreshold \approx Qcrit$$

$$SatCrossSection \approx TransistorSection$$

$$SoftErrorRate \approx \frac{SatCrossSection}{LETthreshold}$$

MOS (BULK)
Parasitic Current Leakage

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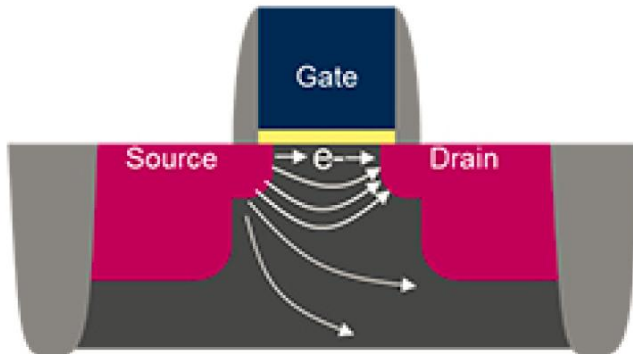
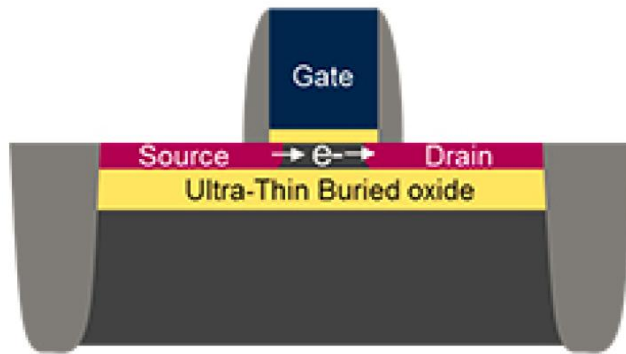


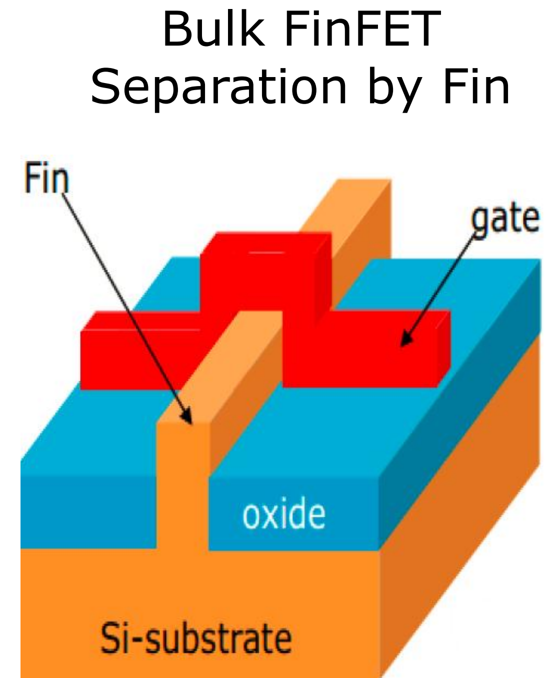
- Scale Integration
- Moore's Law
- 28 nm Barrier
- Parasitic Currents
    - Gate(high K)
    - Bulk
- Mitigation need

New CMOS Technologies FD-SOI, bulk FINFET

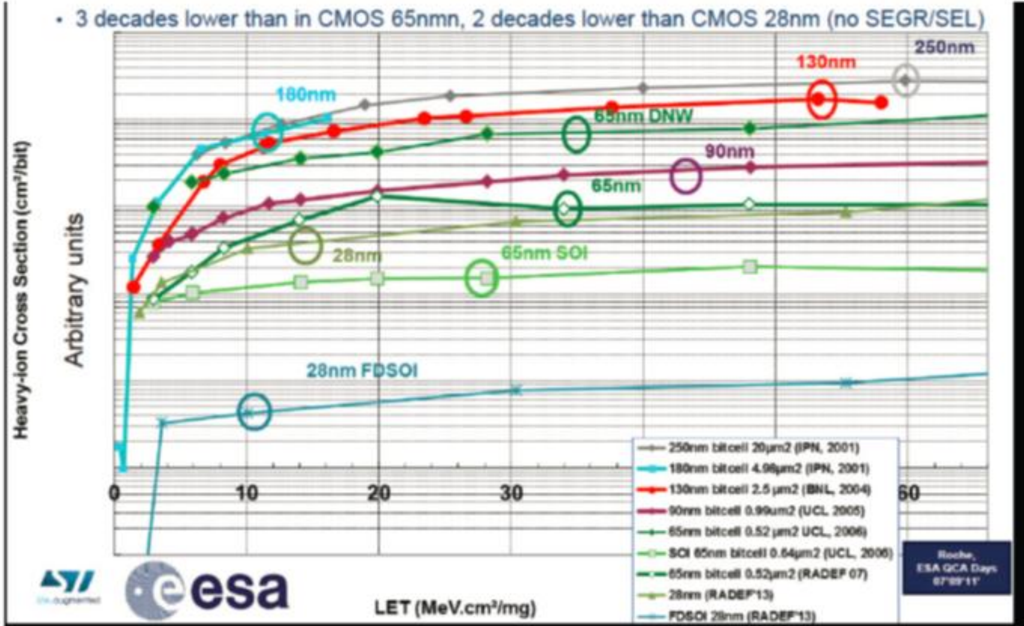


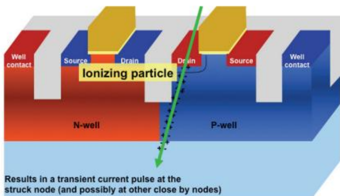
FD-SOI
Burried oxide separation

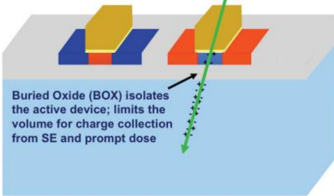
Bulk FinFET
Separation by Fin



Soft errors in FD-SOI





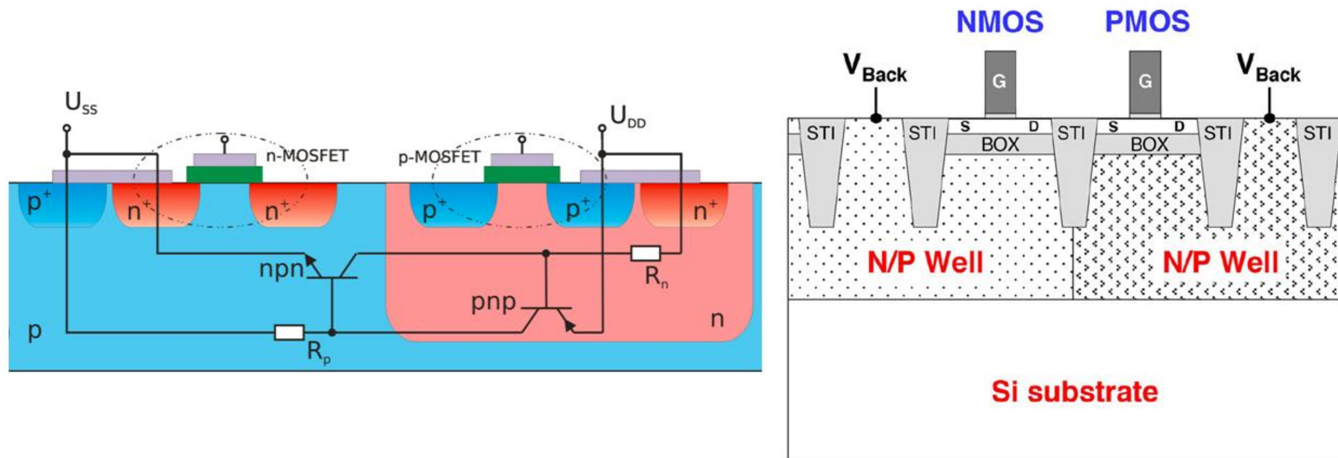


Soft errors in FINFET Core™ i3-5005U

TEST	ERROR	CROSS SECTION [cm^2]		SEU/SEFI RATE [upset/device/day]	MEDIUM TIME TO SEU/SEFI [days]	NUMBER OF SEFIs/YEAR	AVAILABILITY [%]
idle	FATAL (SEFI)		1.E-09	5.10E-08	2.E+07	0.00001770	99.9999999966%
idle	NON-FATAL (SEU)		1.E-09	5.10E-08	2.E+07	0.00001770	99.9999999966%
stress (math + graph)	FATAL (SEFI)	MIN	1.E-08	5.10E-07	2.E+06	0.00017698	99.9999999663%
		MAX	2.E-08	1.02E-06	1.E+06	0.00035396	99.9999999327%
stress (math + graph)	NON-FATAL (SEU)		1.E-08	5.10E-07	2.E+06	0.00017698	99.9999999663%
only math	NON-FATAL (SEU)		3.E-09	1.53E-07	7.E+06	0.00005309	99.9999999899%

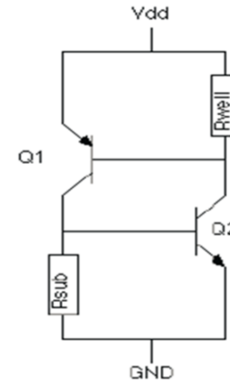
LATCH UP

FD-SOI SEL Tolerance

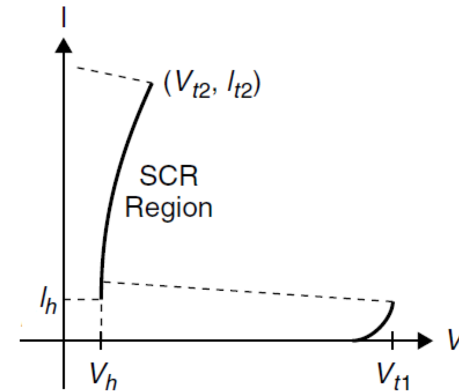


Every SOI technology is intrinsicaly SEL inmune because it doesn't produce parasitic BJTs

Bulk FinFET SEL Tolerance



- Parasitic junctions in bulk
- Vdd range: 0.5 to 1.3 V aprox.
- Vh: 0.8 to 1 V



CONCLUSIONS

- It is clear that scale integration has increased the Total Dose (TIC) tolerance in last generation CMOS devices
- Although some improvement in SEL/SEFI tolerance with scale integration can be seen in the new generation CMOS devices, this can not be consider guaranteed
- FD-SOI technology is intrinsically SEL free. FINFET technology, instead could become SEL free operating at low supply voltages.
- Using these technologies “as is” for space involves less risk from the radiation effects point of view
- There is also a lower risk of not reaching the espected radiation tolerances when upscreening process is used

QUESTIONS?

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